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Date: October 3, 2007 /Stacey Bussey/
Stacey Bussey

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:			
Applicant(s):	Gregory A. Majcher, *et al.*	Examiner:	Bryce P. Bonzo
Serial No:	10/771,891	Art Unit:	2113
Filing Date:	February 4, 2004		

Title: SITUATIONAL AWARE OUTPUT CONFIGURATION AND EXECUTION

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Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

Applicant submits this brief in connection with an appeal of the above-identified patent application. A credit card payment form is filed concurrently herewith in connection with all fees due regarding this appeal brief. In the event any additional fees may be due and/or are not covered by the credit card, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1063 [ALBRP173USA].

I. Real Party in Interest (37 C.F.R. §41.37(c)(1)(i))

The real party in interest in the present appeal is Rockwell Corporation, the assignee of the present application.

II. Related Appeals and Interferences (37 C.F.R. §41.37(c)(1)(ii))

Appellants, appellants' legal representative, and/or the assignee of the present application are not aware of any appeals or interferences which may be related to, will directly affect, or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. Status of Claims (37 C.F.R. §41.37(c)(1)(iii))

Claims 23-31 and 33-44 stand rejected by the Examiner. The rejection of claims 23-31 and 33-44 is being appealed.

IV. Status of Amendments (37 C.F.R. §41.37(c)(1)(iv))

No amendments to the claims were submitted after the Final Office Action. (*See* Applicants' Reply to Final Office Action dated April 19, 2007).

V. Summary of Claimed Subject Matter (37 C.F.R. §41.37(c)(1)(v))

A. Independent Claim 23

Independent claim 23 recites a system that facilitates generating a dynamic output in a state machine, comprising an input component that receives communication, the communication is related to at least one indicator that receives updated status/ event information from the communication (*See* pg. 8, ln. 23 to pg. 9, ln. 11) and a logic function component that defines a logical function using at least one function block and links the logical function with the indicator to define the behavior of an output and selectively provide an output signal according to the logic function and the at least one indicator. (*See* pg. 9, ll. 12-29).

B. Independent Claim 36

Independent claim 36 recites a method to provide a variable output related to received information, comprising accepting an input comprising at least one indicator that indicates updated status/ event information (*See* pg. 7, ll. 1-4), transmitting the input to a logic function, the logic function contains at least one function block (*See* pg. 6, ll. 27-29), associating the at least one indicator with the at least one function block (*See* pg. 6, ln. 26) and providing an output based at least in part upon the at least one indicator and the logic function. (*See* pg. 7, ll. 15-20).

C. Independent Claim 44

Independent claim 44 recites a system that provides an output, comprising means for receiving information regarding associated logical function and status/event indicator components (*See* pg. 9, ll. 5-11), means for determining the status of the associated logical function and status/event indicator components (*See* pg. 9, ll. 7-9), means for selecting an output based on the information received and means for broadcasting an output signal from an output component. (*See* pg. 9, ll. 12-29).

VI. Grounds of Rejection to be Reviewed (37 C.F.R. §41.37(c)(1)(vi))

A. Claims 23-28, 34 and 44 stand rejected under 35 U.S.C. §102(e) as being anticipated by Grieshaber *et al.* (U.S. 6,598,106).

B. Claim 35 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Grieshaber *et al.*

C. Claims 29-33 and 36-43 stand rejected under 35 U.S.C. §103(a) as unpatentable over Grieshaber *et al.* in view of Tentij *et al.* (U.S. 6,513,129).

VII. Argument (37 C.F.R. §41.37(c)(1)(vii))

A. Rejection of Claims 23-28, 34 and 44 Under 35 U.S.C. §102(e)

Claims 23-28, 34 and 44 stand rejected under 35 U.S.C. §102(e) as being anticipated by Grieshaber *et al.* (US 6,598,106). Reversal of this rejection is respectfully requested for at least the following reasons. Grieshaber *et al.* does not disclose, teach or suggest each and every limitation set forth in the subject claims.

> A single prior art reference anticipates a patent claim only if it ***expressly or inherently describes each and every limitation set forth in the patent claim***. *Trintec Industries, Inc. v. Top-U.S.A. Corp.,* 295 F.3d 1292, 63 USPQ2d 1597 (Fed. Cir. 2002); *See Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The ***identical invention must be shown in as complete detail as is contained in the ... claim***. *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) (emphasis added).

Applicants' claimed subject matter relates to mechanisms to enable a user to define output behavior of an output device in a variety of status and/or event circumstances. The user creates a binding between a logical function and the status and/or event indicators. (*See* Summary). In particular, independent claim 23 recites *a system that facilitates generating a dynamic output in a state machine, comprising an input component that receives communication, the communication is related to at least one indicator that receives updated status/event information from the communication* ***and a logic function component that defines a logical function using at least one function block and links the logical function with the indicator to define the behavior of an output and selectively provide an output signal according to the logic function and the at least one indicator***. Independent claim 44 recites similar limitations. Grieshaber *et al.* does not teach or suggest such novel aspects.

Rather Grieshaber *et al.* relates to a dual port enclosure monitor for servicing a dual port Small Computer System Interface (SCSI) bus. (*See* Abstract). The enclosure monitor may communicate with hosts attached to the ports. The hosts can instruct the enclosure monitor to connect or isolate an internal SCSI bus, thus, allowing or disallowing access to SCSI devices

attached to the internal SCSI bus. (*See* Summary). The internal SCSI bus is connected to the host *via* an external SCSI bus of the enclosure monitor. In one disclosed embodiment, the enclosure monitor continuously monitors the internal SCSI bus for errors. If an error is detected that hangs the internal SCSI bus, the enclosure monitor iteratively traverses the attached SCSI devices to determine the offending SCSI device so that it may be isolated. (*See* col. 9, line 49 to col. 10, line 27). Thus, Grieshaber *et al.* relates to detecting and isolating bus faults and is silent regarding a logic function component as recited by the subject claims.

In the Final Office Action dated February 21, 2007, it is contended that Grieshaber *et al.* discloses a logical function at col. 9, line 49 to col. 10, line 27 and item 704 of Fig. 7. Applicants' representative respectfully disagrees. The cited passage relates to detecting a bus fault and/or a bus hang condition. Further, the reference discloses taking steps to isolate the fault. Item 704 of Fig. 7 is a decision element to determine is the bus is hung. This decision is distinct from a logical function with at least one function block and linked to an indicator to define output behavior. This determination is necessary because remedial measures to cure a bus fault cannot occur is the bus is hung. Further, a bus error is not an indicator linked to (*i.e.* input to) a logical function to define output behavior or provide an output signal. Rather, the bus error triggers an iterative loop for isolating the faulting device, thus removing the error.

In view of at least the foregoing, it is readily apparent that the cited document does not disclose, teach or suggest each and every limitation of independent claims 23 and 44 (and the claims that depend therefrom). Accordingly, it is respectfully submitted that this rejection should be reversed.

B. Rejection of Claim 35 Under 35 U.S.C. §103(a)

Claim 35 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Grieshaber *et al.* Reversal of this rejection is requested for at least the following reasons. Claim 35 depends from independent claim 23; and as stated *supra*, Grieshaber *et al.* does not disclose or suggest every limitation set forth in the subject independent claim. Accordingly, this rejection should be reversed.

C. Rejection of Claims 29-33 and 36-42 Under 35 U.S.C. §103(a)

Claims 29-33 and 36-43 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Grieshaber *et al.* in view of Tentij *et al.* (US 6,513,129). It is respectfully requested that this rejection be reversed for at least the following reasons. Grieshaber *et al.* and Tentij *et al.*, individually or in combination, do not teach or suggest each and every element set forth in the subject claim.

> To reject claims in an application under §103, an examiner must establish a *prima facie* case of obviousness. A *prima facie* case of obviousness is established by a showing of three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second there must be a reasonable expectation of success. ***Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.*** *See* MPEP §706.02(j). The teaching or suggestion to make the claimed combination and the reasonable expectation of success must be found in the prior art and not based on the Applicant's disclosure. *See In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) (emphasis added).

In particular, the cited references fail to teach or suggest ***transmitting the input to a logic function, the logic function contains at least one function block, associating the at least one indicator with the at least one function block and providing an output based at least in part upon the at least one indicator and the logic function*** as recited by independent claim 36. As discussed *supra*, Grieshaber *et al.* relates to bus fault detection and isolation. Grieshaber *et al.* does not teach or suggest an association between an indicator and a function block and providing an output based in part on the indicator and the function block. Rather, Grieshaber *et al.* discloses an iterative fault isolation process triggered in response to a detected bus error. Moreover, determining the bus condition is not a logical function with at least one function block and, further, the remedial measures do not provide an output based upon an indicator and the logic function.

In the Final Office Action, Tentij *et al.* is relied upon to make up for the deficiencies of Grieshaber *et al.* with respect to independent claim 36. However, Tentij *et al.* fails to teach or suggest those aspects lacking in Grieshaber *et al.* Tentij *et al.* relates to a fault management

system wherein control objects can be selected for particular alarm incidents such that the selected control object is processed or executed in response to the alarm incident should it occur. (*See* Abstract). Thus, Tentij *et al.* is similar to Grieshaber *et al.* in that a particular routine is executed in response to a detected fault. Tentij *et al.* does not teach or suggest an association between an indicator and a function block and providing an output based in part on the indicator and the function block. Rather, Tentij *et al.* enables a user of the fault management system to select a fault recovery routine that will execute upon detection of a fault. Therefore, Tentij *et al.* fails to cure the deficiencies of Grieshaber *et al.* with respect to the subject claims.

Moreover, the combination of Grieshaber *et al.* and Tentij *et al.*, if possible, would not result in applicants' claimed invention. Rather, the result would be a configurable fault management system for a dual port enclosure monitor servicing a dual port SCIS bus. In particular, a user of the enclosure monitor would be able to alter the fault detection response from the iterative traversal of attached devices as discussed *supra* to some other routine that triggers in response to a detected fault. Thus, such a combination does not teach or suggest all limitations of the claimed subject matter.

Regarding claims 29-33, these claims depend from independent claim 23. As stated *supra*, Grieshaber *et al.* does not disclose, teach or suggest every limitation set forth in the subject independent claim, and Tentij *et al.* fails to cure the deficiencies. Therefore, the rejection of claims 29-33 should be reversed and the claims allowed.

In view of the foregoing, it is readily apparent that Grieschaber *et al.* and Tenji *et al.*, taken alone or in combination, fail to teach or suggest every aspect of the claimed subject matter. Accordingly, reversal of this rejection is respectfully requested.

D. Conclusion

For at least the above reasons, the claims currently under consideration are believed to be patentable over the cited references. Accordingly, it is respectfully requested that the rejections of claims 23-31 and 33-44 be reversed.

If any additional fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [ABLRP173USA].

Respectfully submitted,
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VIII. Claims Appendix (37 C.F.R. §41.37(c)(1)(viii))

1.-22. (Cancelled)

23. A system that facilitates generating a dynamic output in a state machine, comprising:

an input component that receives communication, the communication is related to at least one indicator that receives updated status/ event information from the communication; and

a logic function component that defines a logical function using at least one function block and links the logical function with the indicator to define the behavior of an output and selectively provide an output signal according to the logic function and the at least one indicator.

24. The system of claim 23, the output signal is transmitted to at least one of a process, a machine, a backplane, a bus and a network.

25. The system of claim 23, further comprising a memory component that stores data that is operatively coupled to at least one of the input component, the logic function component and the output component.

26. The system of claim 25, further comprising a processing component that executes instructions within the memory that is operatively coupled to at least one of the input component, the output component and the memory component.

27. The system of claim 26, the processor updates the indicator according to the communication.

28. The system of claim 23, further comprising a closed loop component that receives information from the input component that is operatively coupled to the output component to provide feedback control.

29. The system of claim 23, further comprising a configuration tool that creates an association between the logic function component and the at least one indicator.

30. The system of claim 29, the configuration tool further comprising an intelligence component employed to automatically determine an association between the logic function component and the at least one indicator.

31. The system of claim 29, the configuration tool is one of a computer, a workstation, a handheld PC, a tablet PC, a personal digital assistant and a cell phone.

32. (Cancelled)

33. The system of claim 1, the function block is one of a Boolean operator, a flip-flop, a counter, a timer and an analog function.

34. The system of claim 23, the indicator is at least one of a message connection health indicator, an I/O error indicator, a run/idle indicator, a network error indicator, an I/O point fault indicator, a hardware input indicator, a hardware output indicator, an I/O data indicator, and an output device status indicator.

35. The system of claim 23, the input component further comprises a message buffer component employed to store at least one message and is operatively coupled to at least one of the input component and the logic function component.

36. A method to provide a variable output related to received information, comprising:

accepting an input comprising at least one indicator that indicates updated status/ event information;

transmitting the input to a logic function, the logic function contains at least one function block;

associating the at least one indicator with the at least one function block; and

providing an output based at least in part upon the at least one indicator and the logic function.

37. The method of claim 36, further comprising selecting a function block based at least in part upon the indicator received.

38. The method of claim 36, further comprising associating the at least one indicator with at least one function block *via* a configuration component.

39. The method of claim 36, further comprising receiving the output from the logic function and transmitting the output *via* an output component.

40. The method of claim 36, the at least one indicator is received from an external source on one of a periodic basis, a continuous basis and a one-time basis.

41. The method of claim 36, the at least one indicator is at least one of a status indicator and an event indicator.

42. The method of claim 41, the indicator is at least one of a message connection health indicator, an I/O error indicator, a run/idle indicator, a network error indicator, an I/O point fault indicator, a hardware input indicator, a hardware output indicator, an I/O data indicator, and an output device status indicator.

43. The method of claim 37, the function block is one of a Boolean operator, a flip-flop, a counter, a timer and an analog function.

44. A system that provides an output, comprising:

means for receiving information regarding associated logical function and status/event indicator components;

means for determining the status of the associated logical function and status/event indicator components;

means for selecting an output based on the information received; and

means for broadcasting an output signal from an output component.

IX. Evidence Appendix (37 C.F.R. §41.37(c)(1)(ix))

None.

X. Related Proceedings Appendix (37 C.F.R. §41.37(c)(1)(x))

None.